Electronic Version
Stylesheet Version v1.1.1

# Claims

[c1] What is claimed is:

1.An interface control circuit used in a circuit system for transmitting data, the interface control circuit comprising:

a plurality of I/O pins;

an I/O-pin select sequence table for recording at least an I/O-pin data set; and

an I/O-pin sequence select module for transmitting the data sequentially through the plurality of I/O pins according to the I/O-pin data set.

[c2] 2. The interface control circuit of claim 1 wherein the circuit system is coupled to a second circuit system, and content of the I/O-pin select sequence table conforms to requirements of the second circuit system.

[c3] 3. The interface control circuit of claim 1 further comprising:

a data select sequence table for providing a predetermined sequence; and

a data sequence select module for sequentially transmitting the data according to the predetermined sequence through at least one of the I/O pins.

[c4] 4. The interface control circuit of claim 1 further comprising:
a timing control table for providing a cycle data set; and
a timing control unit for transmitting the data according to the cycle data set.

[c5] 5. The interface control circuit of claim 4 wherein the timing control unit outputs a timing signal according to the cycle data set.

[c6] 6. An interface control circuit for transmitting data, the interface control circuit comprising:
at least an I/O pin;
a data select sequence table for providing a predetermined sequence; and
a data sequence select module for sequentially transmitting the data according to the predetermined sequence through the I/O pin.

[c7] 7. The interface control circuit of claim 6 wherein the circuit system is coupled to a second circuit system, and content of the data select sequence table conforms to requirements of the second circuit system.

[c8] 8. The interface control circuit of claim 6 further comprising:
a timing control table for providing a cycle data set; and

a timing control unit for transmitting the data according to the cycle data set.

[c9] 9. The interface control circuit of claim 8 wherein the timing control unit outputs a timing signal according to the cycle data set.

[c10] 10. An interface control circuit for outputting a timing signal, the interface control circuit comprising:
a timing control table for providing a cycle data set, the cycle data set corresponding to the timing signal; and
a timing control unit for outputting the timing signal according to the cycle data set.

[c11] 11. The interface control circuit of claim 10 wherein the timing control table further comprises a level data set, and the level data set is related to the timing signal.

[c12] 12. The interface control circuit of claim 10 being installed in a circuit system, the circuit system being coupled to at least a second circuit system via the interface control circuit, wherein content of the timing control table conforms to requirements of the second circuit system.

[c13] 13. A method for transmitting data, the method comprising:
determining a predetermined sequence according to a

data select sequence table; and
arranging and transmitting the data according to the predetermined sequence.

[c14] 14. The method of claim 13 further comprising:
determining at least a pin according to a pin select sequence table; and
sequentially transmitting the data via the pin.

[c15] 15. The method of claim 13 further comprising:
sequentially transmitting the data via the pin according to a cycle data set.

[c16] 16. A method for transmitting data, the method comprising:
determining at least a pin according to a pin select sequence table; and
sequentially transmitting the data via the pin.

[c17] 17. The method of claim 16 further comprising:
sequentially transmitting the data via the pin according to a cycle data set.

[c18] 18. A method for outputting a control signal comprising:
determining an output/input timing according to an output/input timing control table; and
outputting the control signal according to the output/input timing.